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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/456,873	MORI, SEIICHI	
	Examiner	Art Unit	
	Leonardo Andujar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

Detailed Action

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 12/09/1998. The certified copy of the priority document has been received.

Claim Rejections - 35 USC § 112

2. Claims 5, 6, 11, 12, 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation that a silicon nitride layer deposited on an oxide layer have trap density lower than a silicon nitride layer which is not previously mention. Therefore, a logic comparison regarding trap density can not be established.

Claims 11 and 12, which depend upon claim 9, recite the limitation that a double-layered silicon nitride layer is contiguous to both a floating gate and a control gate. This limitation is inconsistent with claim 9, which recites the limitation that a silicon oxide layer is contiguous to at least one of the floating gate and the control gate.

Claims 16 and 17, which depend upon claim 14, recite the limitation that a double-layered silicon nitride layer is contiguous to a both floating gate and a control gate. This limitation is inconsistent with claim 14, which recites the limitation that a silicon oxide layer is contiguous to at least one of the floating gate and the control gate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi (5,661,056), Klein et al., Yamada (JP 358106873A) and of Wang et al.

Takeuchi discloses a non-volatile semiconductor memory device (figure 1) including a semiconductor substrate 11 and a memory cell having a floating gate 13 provided through a tunnel insulating layer 12 on the substrate 11. Takeuchi also discloses a control gate 15 provided through an inter- insulating layer 14 on the floating gate 13. The inter-insulating layer 14 includes a silicon oxide layer 14a contiguous to the floating gate 13, and silicon nitride insulating layer over the silicon oxide layer 14a (column 1, lines 37-60).

Takeuchi does not disclose that the silicon nitride insulating layer includes a second silicon nitride layer with a trap density lower than a first silicon nitride layer. Also, Takeuchi does not disclose the hydrogen content. Klein et al. discloses a process to form good quality silicon nitride films by lowering the a hydrogen atomic content near 20% ($4.7x10^{21}$atoms/cm^3). It is know in the art that the trap density is proportional to the hydrogen content, therefore by decreasing the hydrogen content the trap density of the layer is reduced.

Yamada discloses a non-volatile memory device including a first silicon nitride film 104 which can be complemented by forming a second silicon nitride layer over a first silicon nitride layer 104, in order to obtain a desired thickness (abstract). However, Yamada does not disclose the hydrogen content of the second layer. Wang et al. discloses a process to form a silicon nitride film with a hydrogen atomic content of 12.5% (Table I). This type of layer can be used for pre-metal dielectric applications. Moreover, the silicon nitride layer shown by Wang et al. has a trap density lower than the one shown by Klein et al.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the silicon nitride layer of Takeuchi with a hydrogen atomic content of 20% as taught by Klein in order to obtain a good quality silicon nitride films.

Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second layer over the silicon nitide of Takeuchi in view of Klein et al. as taught by Yamada in order to obtain a desired thickness.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the silicon nitride layer of Takeuchi in view of Klein et al. in further view of Yamada with lower hydrogen content by using the process taught by Wang et al. in order to make the layer useful for pre-metal dielectric processes.

In regard claim 4 Takeuchi in view of Klein et al., in further view of Yamada and in further view of Wang et al. do not expressly disclose that the hydrogen content of the second silicon nitride layer is $10^{19}/cm^3$ or less. Although Takeuchi in view of Klein et al.,

in further view of Yamada and in further view of Wang et al. do not teach the exact hydrogen content of the second silicon nitride layer as claimed by Applicant, differences in concentrations are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Applicant's claim 2 does not distinguish over Takeuchi (5,661,056) in view of Klein et al., in further view of Yamada and in further view of Wang et al. combination regardless of the process used to form the second silicon nitride layer, because only the final product is relevant, not the process of making such as plasma-decomposition with silane-series gas and nitrogen gas mixture.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

4. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi (5,661,056) in view of Yamada and in further view of Araki et al.

Takeuchi discloses a non-volatile semiconductor memory device (figure 1) including a semiconductor substrate 11 and a memory cell having a floating gate 13 provided through a tunnel insulating layer 12 on the substrate 11 and a control gate 15 provided through an inter-insulating layer 14 on the floating gate 13. The inter-insulating layer 14 includes a silicon oxide layer 14 contiguous to the floating gate 13 and a first silicon nitride insulating layer 14 located over the silicon oxide layer 14a. The insulator layer 14 is an ONO type. Takeuchi does not disclose that the silicon oxide layer, which is deposited over the floating gate is comprised by a second silicon oxide layer having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less. Yamada discloses a non-volatile memory device including an insulator layers, which is formed by two consecutive layer of the same material. Araki et al. discloses a non-volatile memory device, which include a silicon oxide insulator layer with low hydrogen content. The hydrogen content of the layer is less than 10%.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a second layer of the same material over the silicon oxide layer of Takeuchi as taught by Yamada in order to obtain a desirable thickness.

Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the second silicon nitride layer of Takeuchi in view of Yamada with a low hydrogen content as taught by Araki et al. in order to obtain an

insulator layer with a capacitance corresponding to the design rule of the semiconductor device.

Takeuchi in view of view of Yamada and in further view of Araki et al. do not disclose that the hydrogen content of the second silicon oxide layer is $10^{19}/cm^3$ or less. Although Takeuchi in view of Yamada and in further view of Araki et al. do not teach the exact hydrogen content of the second silicon oxide layer, as claimed by Applicant, differences in concentration are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Applicant's claim 8 does not distinguish over Takeuchi (5,661,056) in view of in view of Yamada and in further view of Araki et al. regardless of the process used to form the silicon oxide layer, because only the final product is relevant, not the process of making such as plasma-decomposition with silane-series gas and nitrogen gas mixture.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious

product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

5. Claims 9, 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi (5,661,056) in view of Klein et al. and in further view of Araki et al. (5,374,847)

Takeuchi discloses a non-volatile semiconductor memory device (figure 1) including a semiconductor substrate 11 and a memory cell having a floating gate 13 which is provided through a tunnel insulating layer 12 on the substrate 11. Also include a control gate 15 provided through an inter-insulating layer 14 which is on the surface of a floating gate 13. The inter-insulating layer 14 includes a silicon oxide layer 14a contiguous to the floating gate 13 and a first silicon nitride insulating layer 14 over the silicon oxide layer 14a. The insulator layer 14 is an ONO layer. A second oxide layer is in contact with the control gate (column 1, lines 37-60). However, Takeuchi does not disclose that the oxide layer 14a has a lower trap density than the silicon nitride layer. Klein et al. discloses a process to form good quality silicon nitride films by lowering the a hydrogen atomic content near 20% ($4.7x10^{21}$atoms/cm^3). It is know in the art that the trap density is proportional to the hydrogen content, therefore by decreasing the hydrogen content the trap density of the layer is reduced. Araki et al. discloses a non-volatile semiconductor memory device with a silicone oxide layer having a hydrogen content not greater than10% (column 6, line 9).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to make a silicon nitride layer of Takeuchi with a hydrogen atomic content of 20% in order to obtain a good quality silicon nitride films, as taught by Klein et al. Also, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the silicon oxide layer of Takeuchi in view of Klein et al. with a hydrogen content not greater than 10 %, as taught by Araki et al., because a low hydrogen content is desirable to achieve a stable threshold voltage. Therefore, the silicon oxide layer will have a lower trap density than the silicon nitride, because the trap density is proportional to the hydrogen content.

In regards to claim 14 Takeuchi in view of Klein et al. and in further view of Araki et al. lacks or do not expressly disclose that the hydrogen content of the silicon oxide layer is $10^{19}/cm^3$ or less. Although, Takeuchi in view of Klein et al. and in further view of Araki et al. do not teach the exact hydrogen content of the silicon oxide layer as claimed by Applicant, differences in concentration are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Applicant's claims 9 and 10 do not distinguish over Takeuchi (5,661,056) in view of Klein et al. and in further view of Araki et al. regardless of the process used to form the silicon nitride layers, because only the final product is relevant, not the process of making such as plasma-decomposition with silane-series gas and nitrogen gas mixture, and CVD.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

6. Claim 13, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi in view of Klein et al and in further view of Araki et al. as applied to claim 14 above, and further in view of Tomioka et al. (5,793,081).

Takeuchi in view of Klein et al and in further view of Araki et al. disclose a non volatile semiconductor memory device having an insulation layer composed of a silicon oxide and a nitride layer. They do not disclose the silicon nitride layer is provide only on the side contiguous to the floating gate or the silicon oxide layer having a stacked layer consisting of silicon nitride and silicon oxide. Tomioka et al. disclose a nonvolatile semiconductor storage device (2a-k) having an ONO insulator layer that can be substituted by an ONON type (column 1, line 7).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to substitute the ONO insulator layer of Takeuchi in view of Klein et

al. and in further view of Araki et al. by an ONON type layer, as taught by Tomioka et al. in order to obtain an insulator layer with a capacitance corresponding to the design rule of the semiconductor device. In this case only the floating gate will be in contact with the floating gate.

Applicant's claims 13, 15 and 18 do not distinguish over Takeuchi in view of Klein et al., in further view of Araki et al. and in further view of Tomioka et al. combination regardless of the process used to form the silicon oxide layer or silicon nitride layer, because only the final product is relevant, not the process of making such as plasma-decomposition with silane-series gas and nitrogen gas mixture, and CVD.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Takeuchi (5,907,183) discloses non-volatile semiconductor

device having a NON inter-insulator layer and other structures related to the instant invention. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2814 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andujar** at **(703) 308-0080** and between the hours of 9:00 AM to 5:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703)305-3900**

The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/314-317, 324,325, 406, 410 and 411	3/21/01
Electronic Database(s): East (USPAT)	3/21/01

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3/21/01

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